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Patterned Quantum Dot Photosensitive FETs for Medium Frequency Optoelectronics

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The use of colloidal quantum dots (CQDs) as active layers for the transistors in integrated circuits is often impeded by the poor compatibility of CQDs films with the standard lithographic processing. Successful patterning of tetrabutylammonium iodide-treated PbS CQDs films is demonstrated on (3-aminopropyl)triethoxysilane (APTES) functionalized glass or aluminum oxide surfaces, using lithography. Short-channel (4 µm) field-effect transistors (FETs) with patterned gate electrode and patterned CQDs film as active layer with electron mobility of 0.1 $cm^2 V^{-1} s^{-1}$, threshold voltage of –0.29 V, and cutoff frequency of 400 kHz are demonstrated. Furthermore, the lithographic processing does not compromise the optical properties of the film, as evidenced by the photoresponse measurements of the FETs (11.6 mA W^{-1} at 920 nm and 26.7 mA W^{-1} at 440 nm). These results further demonstrate CQDs as a potential material for optoelectronic applications, where medium frequency operation is required.

1. Introduction

Colloidal quantum dots (CQDs) are semiconducting nanocrystals with utterly fascinating physical properties that recently triggered great attention from the optoelectronic community.[1–3] One of their most interesting properties is the size-dependent bandgap, which allows tuning the absorption of the CQDs merely by changing their size. Along with inexpensive and well-established synthesis, the solution processing, the possibility of deposition over large-area and flexible substrates have determined the use of CQDs in solar cells, light-emitting diodes, photodetectors, water splitting photoelectrodes, field effect transistors, etc.[4–8] Among others, PbS CQDs are used successfully in solar cells and photodetectors due to strong and broad absorption, going from the visible to the near-infrared range.[9,10] Furthermore, high performance field-effect transistors and basic logic elements were demonstrated with this material.[11,12]

However, a number of issues are often associated with the fabrication of CQDs thin-film devices. As synthesized, CQDs are commonly capped with long aliphatic ligands, such as oleic acid (OA), to ensure a stable colloidal dispersion in nonpolar solvents.[13] These molecules form an insulating barrier surrounding CQDs, strongly hindering the charge transport between quantum dots when they are assembled in a thin film. One approach to overcome this obstacle is the layer-by-layer spin-coating with subsequent ligand exchange to smaller entities (for example, using tetrabutylammonium iodide (TBAI) treatment).[11] Such ligand exchange causes large volume reduction with consequent formation of cracks in the film and poor adhesion to hydrophilic surfaces.[12] Additionally, unprotected PbS CQDs films show reversible degradation of electron transport upon exposure to air.[14] Thermal annealing under inert atmosphere can restore the electron transport; however, when performed at high temperature and for long time, it leads to sintering of CQDs, compromising the quantum confinement, with consequent degradation of important device parameters.[15]

The aforementioned complications and the sensitivity of quantum dots solids to air, solvents, and thermal treatments often withhold their use in highly integrated circuits, generally made by optical lithography. However, patterning of the active layer is often a necessary step to reduce parasitic resistances and capacitances, which is vitally important for high-performance and high-frequency device fabrication. For example, in a field effect transistor, limiting the semiconducting layer only to the channel region decreases the gate leakage and cross-currents when the transistor is part of an integrated circuit; patterning

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of the gate electrode decreases its overlap with source/drain contacts, thus reducing the parasitic capacitance.

Herein we demonstrate TBAI-treated PbS CQDs FETs, fabricated by multiple lithography steps on a flexible polymeric substrate. First, we demonstrate that, with a proper surface treatment with (3-aminopropyl)triethoxysilane (APTES), PbS CQDs film sticks to the glass/alumina surface strongly enough to sustain wet etching without any delaminating or cracking. Such patterned PbS CQDs films were further used as an active layer in patterned-gate FETs. Short-channel devices, which show prevailing electron transport with the mean effective mobility value of 0.1 $cm^2\ V^{-1}\ s^{-1}$ and the threshold voltage of –0.29 V, were obtained. These are the first PbS CQDs FETs, for which the cut-off frequency was tested and demonstrated. The measured value of 400 kHz is in agreement with the theoretically predicted value of 500 kHz. To demonstrate that the multiple fabrication steps performed in air do not compromise the optical properties of the film, we study the photoresponse of the devices. The values (11.6 mA W^{-1} at 920 nm and 26.7 mA W^{-1} at 440 nm) of the responsivity spectra shows that lithographic etching has practically no influence on the physical properties of the CQD assembly. These results further demonstrate the great potential of CQD solids as highly integratable optoelectronic material.

2. Results and Discussion

CQDs films were deposited on glass/alumina surfaces functionalized with APTES. The films were formed via a typical layer-by-layer spin-coating technique of OA-capped PbS with subsequent ligand exchange with TBAI. Obtained films were patterned via wet etching and further used as an active layer for FETs, as it is demonstrated in **Figure 1**. Figure 1a shows an optical image of a TBAI-treated PbS film, patterned with the university logo using a mask-less lithography technique. This is the first time that the etching of a ligand exchanged CQD film is reported; therefore, it is important to demonstrate the quality of the pattern. The atomic force microscopy (AFM) images show a film of ≈63 nm thickness and root mean square (RMS) roughness of 4.23 nm, with no pinholes or cracks (see Figure S1 in the Supporting Information). To prove the quality of the material removal upon etching, the AFM scan of one of the edges of the CQDs film logo is depicted in Figure 1b, where the sharp and clean profile is evident. It is important to underline that experiments where the CQDs are deposited directly on the untreated substrate surface (covered with hydroxyl groups) gave rise to partial or complete delamination of the film during resist removal process. The delamination totally disappears when the CQDs are deposited on APTES-functionalized glass substrate or aluminum oxide gate dielectric (see Experimental Section).

The schematics of the FETs, utilizing patterned PbS CQDs films, is shown in Figure 1c, and the corresponding microscopy image in Figure 1d. Devices were fabricated on a flexible thermally-cured polyimide films, spin-coated on a 5 × 5 cm^2 glass substrate. On the polyimide, patterned gate electrodes are lithographically defined in order to decrease parasitic capacitance, caused by the overlap of the gate and the source/drain electrodes. On the patterned gate electrode a 100 nm thick layer of Al_2O_3 is grown by atomic layer deposition (ALD). PbS QDs film is deposited and treated with TBAI as described in the experimental section and reported earlier. This layer is also patterned and limited to the channel region in order to minimize gate leakage current and parasitic capacitances. On top of the active layer, source and drain electrodes are lithographically defined.

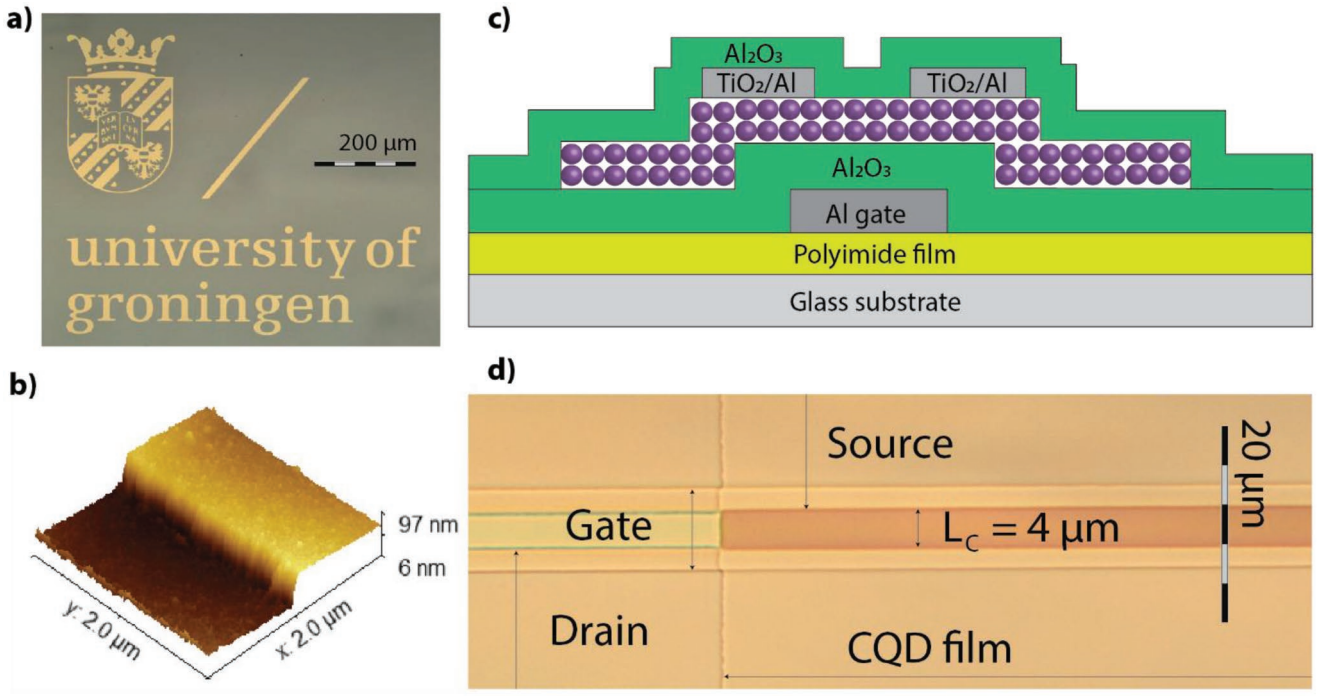

Figure 1. Etched CQDs film for FETs. a) Optical microscopy image of patterned CQDs film. b) AFM profile of an edge of the patterned CQDs film. c) Schematic structure and d) optical microscopy image of CQDs FET with patterned gate and active layer.

After all the fabrication steps the substrate was encapsulated with a layer of aluminum oxide grown by ALD, to increase the stability of the device in air. The design of the photomasks used for the lithography allowed fabrication of FETs with different channel length from 4 µm for high-frequency operation (short-channel FET) to 7, 12, 22, 52, and 102 µm to estimate the contact resistance using the transfer line method (TLM).[16]

The transfer and output curves of the FETs, made in our first experiments, showed high injection barrier for electrons (see Figure S2 in the Supporting Information). This is determined by the use of a tetramethylammonium hydroxide (TMAOH) based developer during the photoresist patterning, which we found can modify the TBAI-treated QDs film by substituting the I^- ligands on the surface of CQDs with OH^- groups. This hypothesis of the I^-–OH^- substitution was verified by comparing TBAI-treated with TMAOH-treated and subsequent TBAI/TMAOH treated PbS QDs FETs. The transfer curves of TBAI/TMAOH treated PbS QDs FETs are almost identical to the one of the purely TMAOH-treated FETs, showing larger threshold voltage than the classical TBAI-treated FETs (see Figure S3 in the Supporting Information). In order to remove the undesired electron barrier, a thin layer of TiO_2 (≈6 nm) was deposited by ALD before the deposition of aluminum, which will form the source and drain electrodes. We speculate that the highly reactive titanium tetrachloride (the ALD precursor) successfully reacts with OH^- groups on CQDs surfaces during the ALD process, creating a titania shell and efficiently removing the injection barrier for electrons.

The output and transfer characteristics of a short-channel PbS QDs FET with TiO_2/Al contacts are shown in **Figure 2**. After fabrication and encapsulation, generally, poor transport properties with low current and large hysteresis are obtained; however, after sufficient thermal annealing on a hot plate (typically, 2 h at 120 °C), the behavior improves largely (see Figure S4 in the Supporting Information) and properties as the one in Figure 2 can be measured.

The electron current in the output characteristics shown in Figure 2a show negligible hysteresis and clear linear/saturation regime. For the hole channel, the current is much smaller, and a hysteretic behavior appears and increases with increasing gate voltage. In agreement with previous reports, this behavior can be explained by the presence of charge traps for holes, injected through the low-work-function TiO_2/Al contacts.[17] Figure 2b shows transfer curves of the FET, confirming the strong n-type properties the minor hole injection for higher drain voltages, which affect the off-current of the device and decrease the on–off ratio from 10^5 for 1 V drain bias to 10^4 for 12 V bias. The effective electron field-effect mobility (μ_{eff}), extracted from the slope of the transfer curve in linear mode, is 0.10 $cm^2\ V^{-1}\ s^{-1}$ with a standard deviation of 0.01 $cm^2\ V^{-1}\ s^{-1}$; the threshold voltage V_{TH} is −0.29 ± 0.01 V (See Figure S5 in the Supporting Information for more statistics). Interestingly, the effective mobility does not show monotonic decrease with decreasing channel length, indicating low contact resistance that is crucial for the high-frequency operation of FETs. Devices with longer channels, up to L_C = 12 µm, show slightly higher effective mobility (17% increase) compared to the short-channel ones; however, the mobility decreases again as channel length further increases, going back to 0.1 $cm^2\ V^{-1}\ s^{-1}$ for 102 µm channel.

For high-frequency operation, besides high charge carrier mobility and low contact resistance, a low gate leakage current and low parasitic capacitance are extremely important. The cutoff frequency, which is the maximal operational frequency of an individual FET, can be approximated with the following expression[18]

$$f_T = \frac{\mu_{eff} V_D}{2\pi L_C (L_C + L_{OV})}$$

Where V_D is the drain voltage, L_C is the channel length, and L_{OV} is the total overlap of the gate electrode with source and drain electrodes. For our short channel devices, for V_D = 10 V bias, μ_{eff} = 0.1 $cm^2\ V^{-1}\ s^{-1}$, L_C = 4 µm, $L_C + L_{OV}$ = 8 µm, which gives a cutoff frequency f_T = 500 kHz.

The cutoff frequency is the frequency, at which the gate current is equal to the drain current, and is, therefore, the

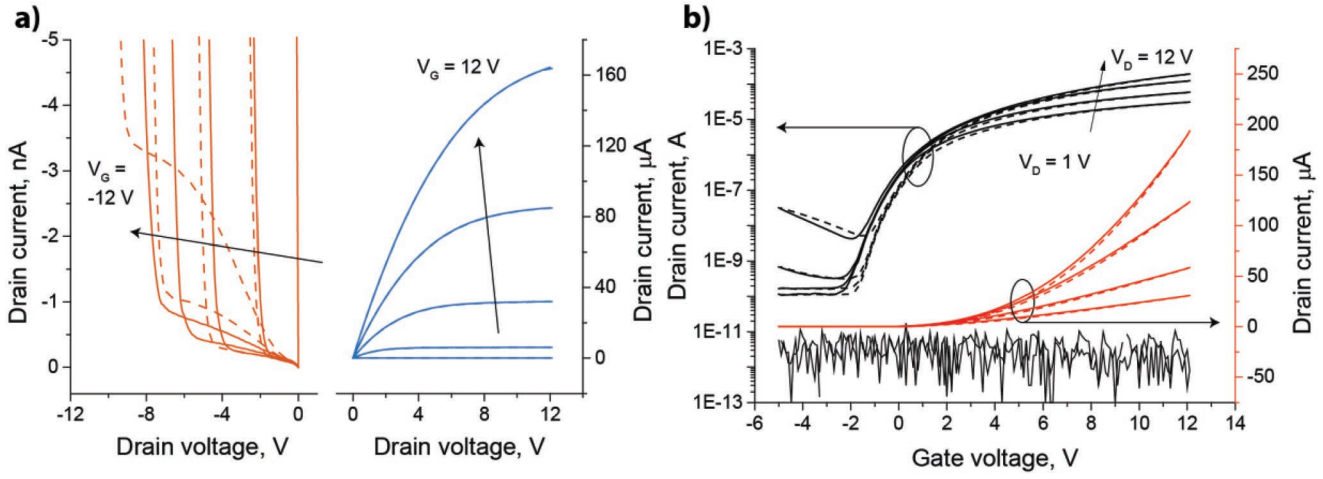

Figure 2. Electrical characteristics of a short-channel CQDs FET. a) Output characteristics of a short-channel (4 µm) CQDs FET measured for n-channel (right) and p-channel (left). b) Transfer characteristics of CQDs FET measured for drain voltages of 1, 2, 5, and 12 V, plotted in linear and logarithmic scale. The gate leakage current is plotted as a black curve in logarithmic scale. Dashed curves illustrate reverse hysteresis branches for both output and transfer curves.

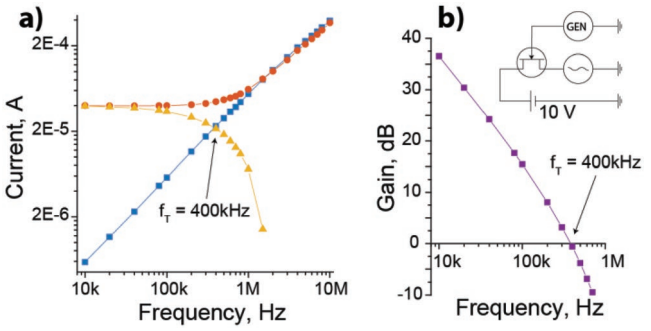

Figure 3. Cutoff frequency measurement for short-channel CQDs FET. a) Source current (red circles), gate current (blue squares), and calculated drain current (yellow triangles) for a short-channel CQDs FET for different frequency of the gate voltage signal. The connection scheme for the frequency measurements is shown in the inset. b) The gain, calculated from the data depicted in inset (a), of a short-channel CQDs FET.

frequency at which the current gain becomes zero.[18] In our short-channel PbS QDs FET, the cut-off frequency was measured using a simple setup, the schematics of which is shown in the inset of **Figure 3**a. A constant bias voltage of 10 V and a high-frequency sinusoidal signal with 1 V RMS amplitude was applied to the gate of the FET. A 50 Ω- terminated oscilloscope was connected to the source electrode and was used to monitor the source current of the FET. When the drain bias voltage is set to 0 V, the oscilloscope signal is merely equal to the gate current (blue squares); when the drain bias is set to 10 V, the source current is equal to the sum of the gate current and the drain current (red circles). The drain current was calculated as the difference between the gate current and the source current under the aforementioned biasing conditions (yellow triangles). As it is shown in Figure 3a, the gate current is increasing proportionally to the frequency of the signal, following a plain capacitor model. The drain current is stable up to 100 kHz, when it starts decreasing. Both these trends cause the decrease of the gain (Figure 3b), which is equal to zero at f_T = 400 kHz. This value is slightly lower than the calculated 500 KHz; we believe part of this discrepancy could be due to our experimental setup, which use an oscilloscope instead of current probes.[18]

It is important to underline that these are the first ever-reported measurements of the cutoff frequency of CQDs FETs, which were made possible by the patterning of the CQD layer by a standard lithographic process and by the optimization of the device structure and the sample encapsulation. The lithographic patterning allows reducing the parasitic capacitance while the optimization of the device structure and the transistor encapsulation is fundamental for obtaining hysteresis-free device characteristics. It should be noted, that after the AC/DC gate bias stress caused during cut-off frequency measurements, the device did not show a decrease of the on-current or significant threshold voltage shift.

Since PbS CQDs can absorb efficiently near-infrared light, we have tested our PbS CQDs FET as possible in-chip photodetectors. The results of the measurements are depicted in **Figure 4**. First, the device was connected and measured in phototransistor mode (Figure 4a). The drain voltage was fixed at 1 V and the transfer curve was measured in dark (blue squares) and under white light (yellow circles). Second, the device was measured in a photodiode mode, connected accordingly to the schematics in Figure 4b. The photodiode shows good rectification ratio of 10^4 at $V_{DD} = \pm 3$ V. Under white light illumination both photodiode and phototransistor measurements yield ≈2 orders of magnitude increase of the current. The external quantum efficiency spectrum of the phototransistor was measured for $V_D = 5$ V and $V_G = -4$ V, and is depicted in Figure 4c. For the measurements, the channel surface of total area of 8×10^{-9} m^2 was illuminated by light passing through a set of color filters, the number of photons for each wavelength is measured with calibrated photodetectors. The responsivity shape resembles a typical absorption curve of TBAI-treated PbS CQDs film, with a visible excitonic peak at ≈920 nm. This value is considerably shifted towards the red compared to the excitonic peak of the

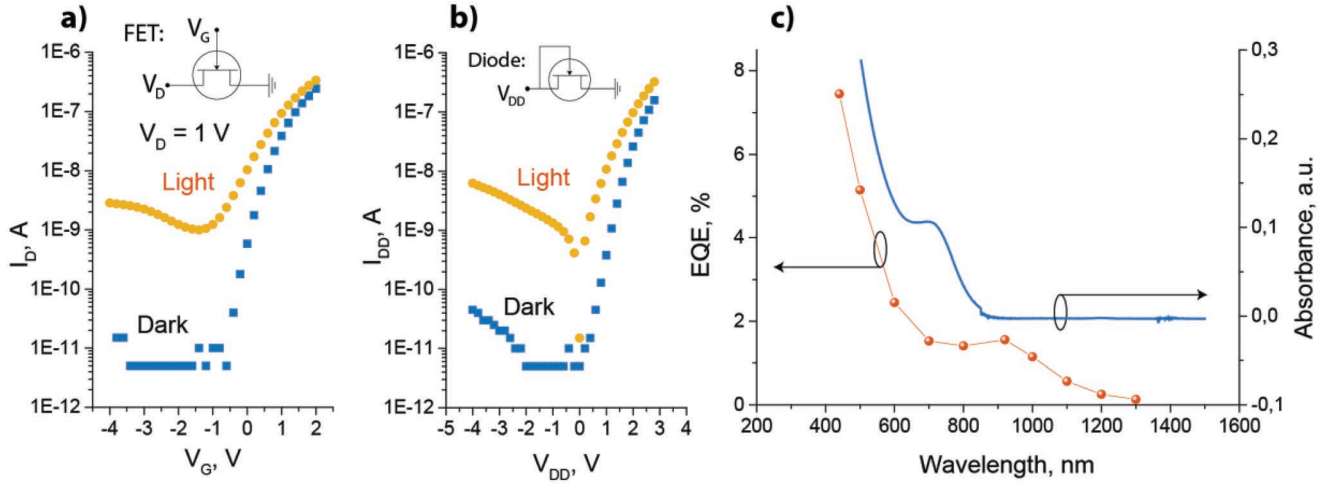

Figure 4. CQDs FET as a photodetector. a) Transfer curve of a CQDs FET for 1 V drain bias measured in dark (blue squares) and under illumination (yellow circles). b) Current–voltage curve of a CQDs FET connected as a diode in the dark (blue squares) and under illumination (yellow circles). c) The external quantum efficiency of a CQDs FET measured for 5 V drain bias and −4 V gate bias (red circles). The blue curve is the absorption spectra of the CQDs in solution.

OA-capped PbS CQDs in solution, used for the fabrication of the device, that is at 700 nm. Therefore, the thermal annealing was not only instrumental to improving the charge transfer properties of the FETs but also caused partial sintering of the nanoparticles. The values of the responsivity reach 11.6 mA W^{-1} at 920 nm and 26.7 mA W^{-1} at 440 nm, and depends on the biasing conditions of the device. In typical photogate-based devices, the photogenerated charges induce the effective shift of the threshold voltage leading to high gain values and slow time-dependent photoresponse.[19–21] This gain mechanism is absent in our device architecture, and the photoresponse is caused by the direct contribution of the photogenerated carriers to the conductivity of the channel in the depleted state, thus limiting the external quantum efficiency (EQE) of the light conversion (which is the number of transported electrons per the number of incident photons) to the values smaller than unity (1.5% at 920 nm and 7.5% at 440 nm) but with the advantage of a highly responsive device.[22] Therefore, for practical applications requiring efficient and fast light detection, an amplification circuit might be required, which can be fabricated from similar PbS QD FETs.[23]

3. Conclusion

In this report, we demonstrate CQDs FETs with effective mobilities of 0.1 cm^2 V^{-1} s^{-1} and cutoff frequency of 400 kHz. CQDs films on APTES-functionalized aluminum oxide or glass surfaces were patterned using lithography. To remove the electron injection barrier from source/drain electrodes into the CQDs film, a thin layer of low-temperature ALD-grown TiO_2 was deposited before aluminum deposition. Thermal annealing is needed to improve the transport properties of the FETs after fabrication that leads to partial sintering of the film; however, partial quantum confinement was preserved, what was confirmed by the responsivity measurements of a phototransistor. The responsivity shape resembles the typical absorption spectrum of TBAI-treated PbS film with the first excitonic peak at 920 nm. These findings show that PbS CQDs films are fully compatible with standard lithography operations and therefore can be used as a part of an integrated circuits working in the medium frequency range. Additionally, PbS CQDs FETs show photoresponse for near-infrared light and, possibly in combination with an amplification circuit integrated from similar FETs, can be used as in-chip photosensors, e.g., for optical communication.

4. Experimental Section

PbS CQDs Synthesis: PbS CQDs were synthesized following an up-scaled hot-injection technique developed by Yarema et al.[24] Briefly, PbO (18 g, 80 mmol) was mixed with 50 mL of oleic acid and 750 mL of 1-octadecene in the 2 L three-neck flask. The addition funnel with 8.4 mL (40 mmol) of bis(trimethylsilyl)sulfide and 400 mL of dried 1-octadecene was connected to the flask. Lead oxide solution was degassed at 120 °C for 2 h. After that flask was refilled with nitrogen and temperature was settled to 82 °C. Prior to injection, the heating mantle was removed and a vacuum was applied until the pressure reaches 1–10 mbar. After that, the vacuum valve was closed and the stopcock of the addition funnel was opened resulting in fast injection of the sulfur precursor. Solution was allowed to cool down naturally for 8 min. PbS CQDs were washed three times with hexane/ethanol solvent/nonsolvent pair and finally redissolved in hexane.

Bottom Gate FET Substrate Fabrication: A polyimide film was spin-casted on a glass substrate from polyimide precursor–polyamic acid U-Varnish S (UBE Industries) and thermally cured at 450 °C for 10 min. After cooling down, an aluminum thin film (45 nm) was deposited via thermal evaporation. Bottom gate electrodes were patterned via lithography using the high-resolution image-reversal photoresist AZ 5214 E (MicroChemicals) in positive mode, and etching of the aluminum by TechniEtch Al80 (MicroChemicals). After resist removal, the substrates were treated with O_2 plasma for 3 min to remove residual photoresist and to enlarge the amount of native aluminum oxide on the surface. The gate dielectric, Al_2O_3 was deposited using a low temperature (100 °C) ALD process (ALD deposition system R200 Advanced system, Picosun) using trimethyl aluminum (TMA) and water as precursors. The thickness of the aluminum oxide was ≈100 nm (1000 ALD cycles + native oxide layer), corresponding to the gate capacitance of 80 nF cm^{-2} (measured using an impedance meter in a flat capacitor configuration).

APTES Functionalization of the Surfaces: Aluminum oxide and glass surfaces were functionalized using APTES prior PbS CQDs film casting for better adhesion. APTES was dissolved in toluene (1 µL per 20 mL), and the substrates were immersed in the solution. For APTES self-assembled monolayer (SAM) formation, the solution was heated to 100 °C in a nitrogen atmosphere for 1 h; the substrates were rinsed with toluene and dried on a hot plate at 120 °C afterward.

TBAI-Treated PbS CQDs Film Deposition: TBAI-treated PbS CQDs were deposited via layer-by-layer spin-coating from 20 mg mL^{-1} OA-capped PbS CQDs solution in hexane and subsequent ligand-exchanged using a puddle treatment by 11 mg mL^{-1} TBAI solution in methanol for 35 s followed by a double washing step with pure methanol and spin-drying. The procedure was repeated three times to get TBAI-treated PbS CQDs film of ≈63 nm. At the end of the deposition process the substrate was annealed at 125C for 1 min.

TBAI-Treated PbS CQDs Film Patterning: The patterning of the CQDs film was done in air using lithography photomasks or a maskless exposure system (SmartPrint, SmartForce Technologies). The patterns were defined using AZ nLof 2020 photoresist (MicroChemicals) and wet-etching was done by immersing the substrates in 1×10^{-3} M water solution of HCl for ≈1 min. After washing with demi water, the resist layer was removed by sonication in acetone and rinsed with isopropanol. The substrate was dried in vacuum for 30 min before the next lithography step.

Top Contact Fabrication and Encapsulation of FETs: For the top contact deposition, the electrodes were patterned with AZ 5214 E photoresist (positive mode). The substrate was moved into the ALD chamber, and TiO_2 was deposited at 100 °C from titanium tetrachloride ($TiCl_4$) and water (120 cycles). The sample was them move to the vacuum chamber of the thermal evaporator where 45 nm aluminum were deposited. The lift-off was done by sonicating the substrate in acetone for 15 min and subsequent rinsing with isopropanol. After that, the substrate was moved in an N_2—filled glovebox and annealed on a hot-plate at 125 °C for 2 h. For encapsulation, ≈50 nm of aluminum oxide was deposited using the above-described ALD process.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

cutoff-frequency, field-effect transistors, photodetection, quantum dots

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